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(54) **A/D CONVERTER AND SOLID-STATE IMAGING APPARATUS WITH OFFSET VOLTAGE CORRECTION**

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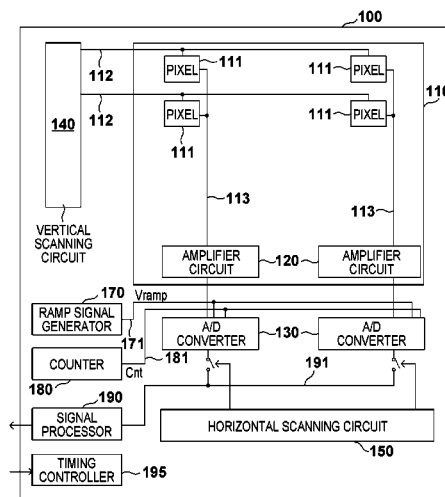
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See application file for complete search history.

ABSTRACT

Provided is an A/D converter including an input terminal, a reference signal line for supplying a reference signal which changes temporally, a comparator, a correction capacitor connected to an inverting input terminal of the comparator; and an output circuit which outputs digital data corresponding to an analog signal input to the input terminal. In a first state in which a total voltage of a first analog signal and an offset voltage of the comparator is held in the correction capacitor, a second analog signal input to the input terminal is supplied to a non-inverting input terminal of the comparator, and the second analog signal or the total voltage is changed using the reference signal, thereby outputting, from the output circuit, digital data.

11 Claims, 8 Drawing Sheets



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FIG. 1

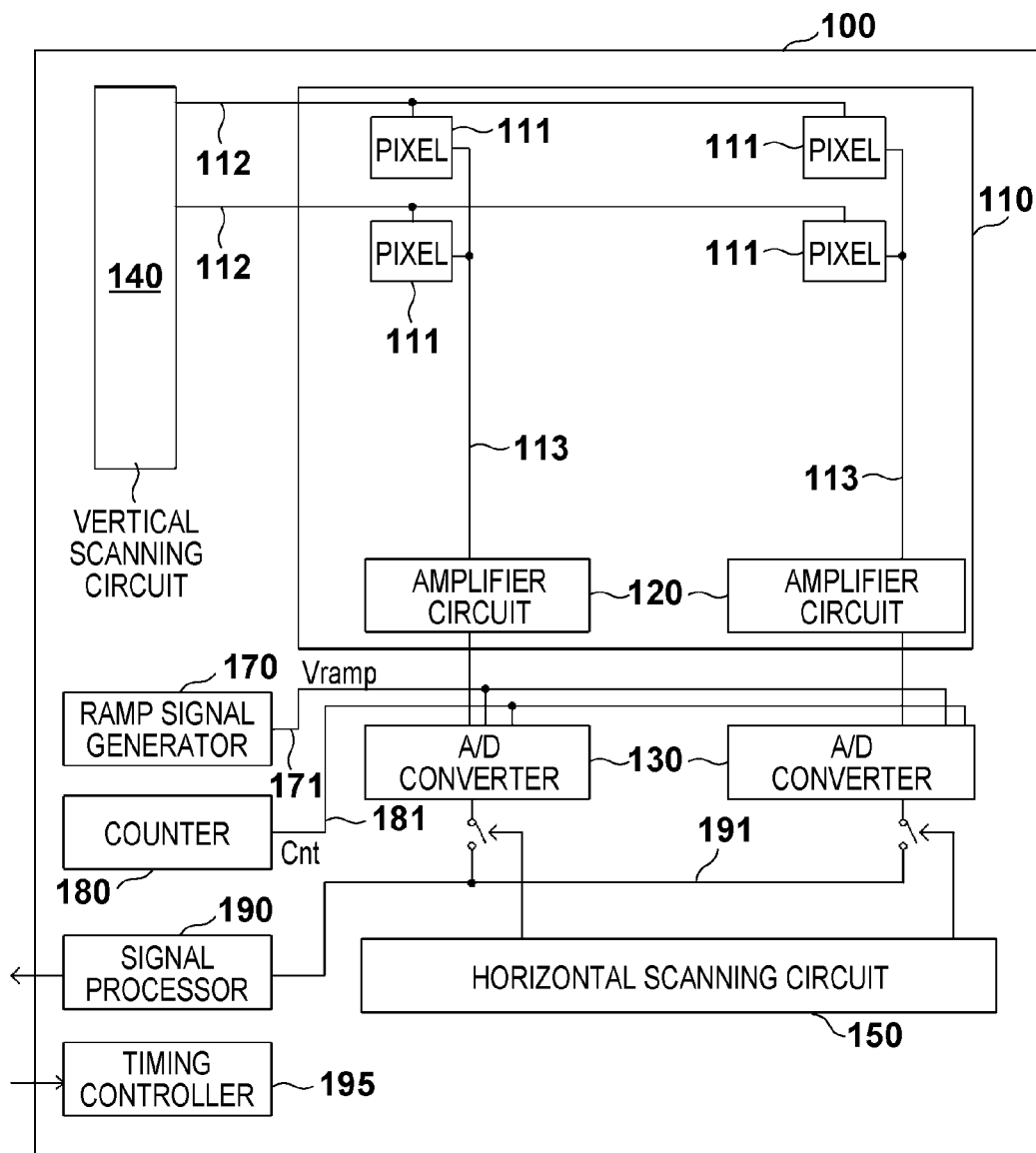


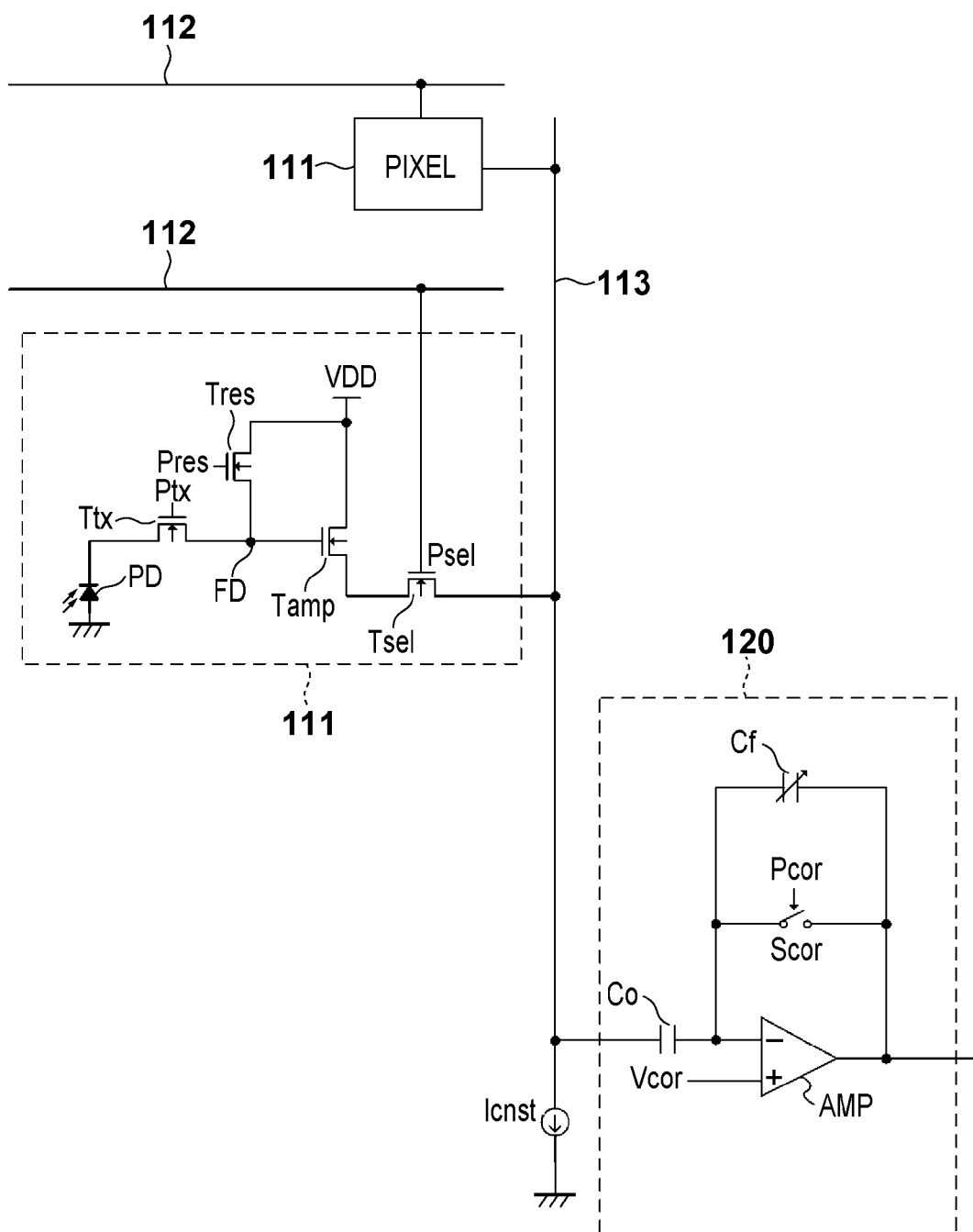
FIG. 2

FIG. 3

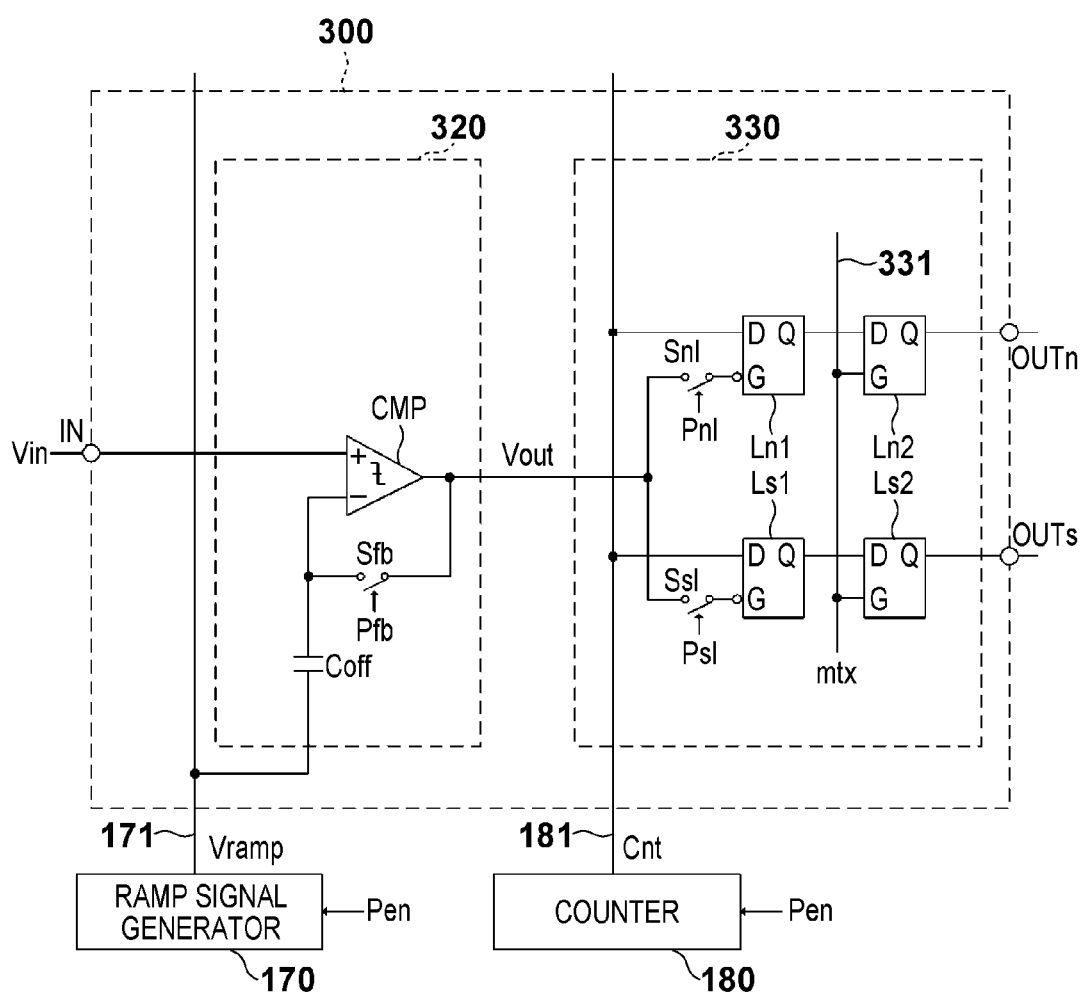


FIG. 4

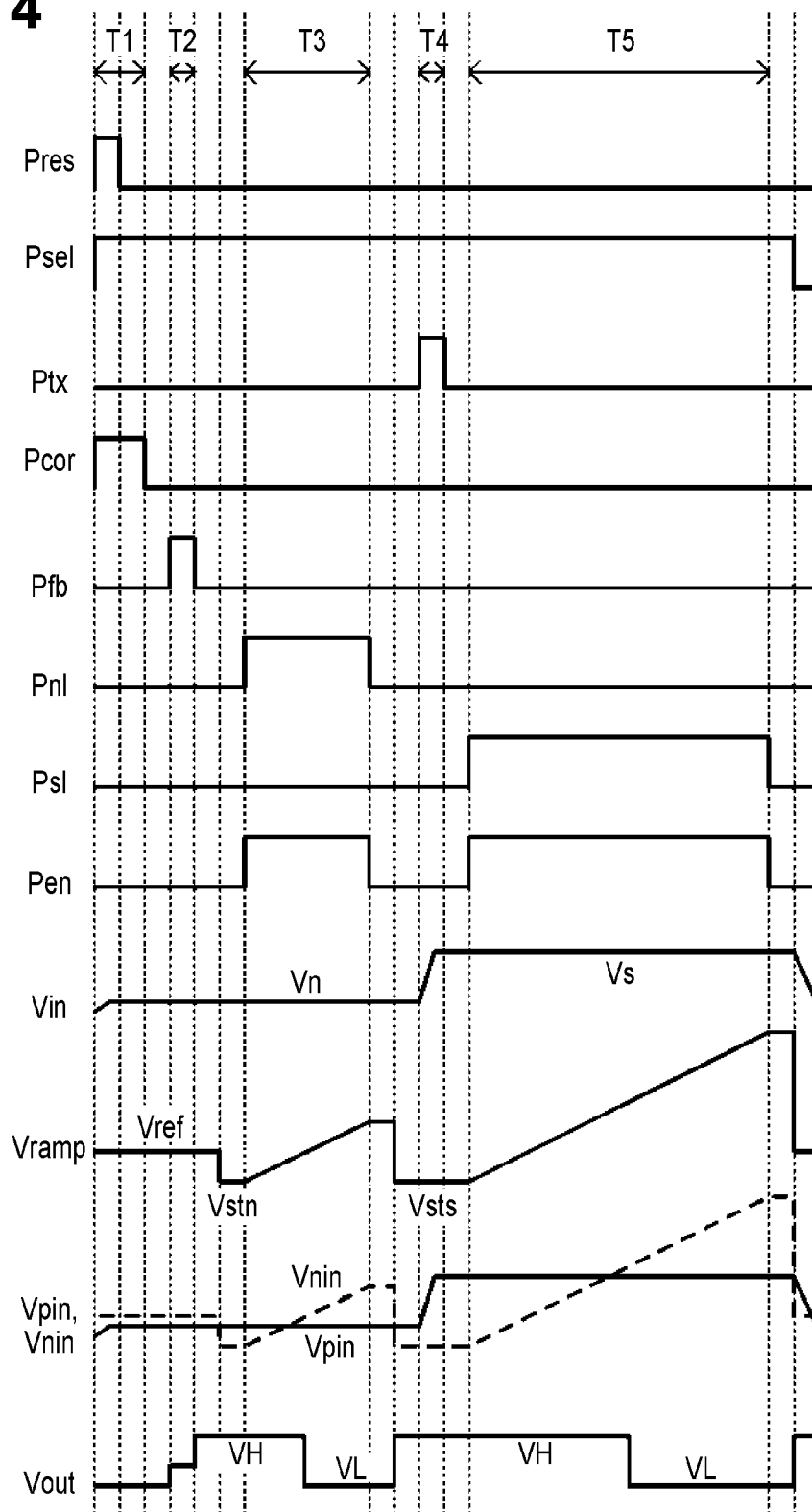


FIG. 5

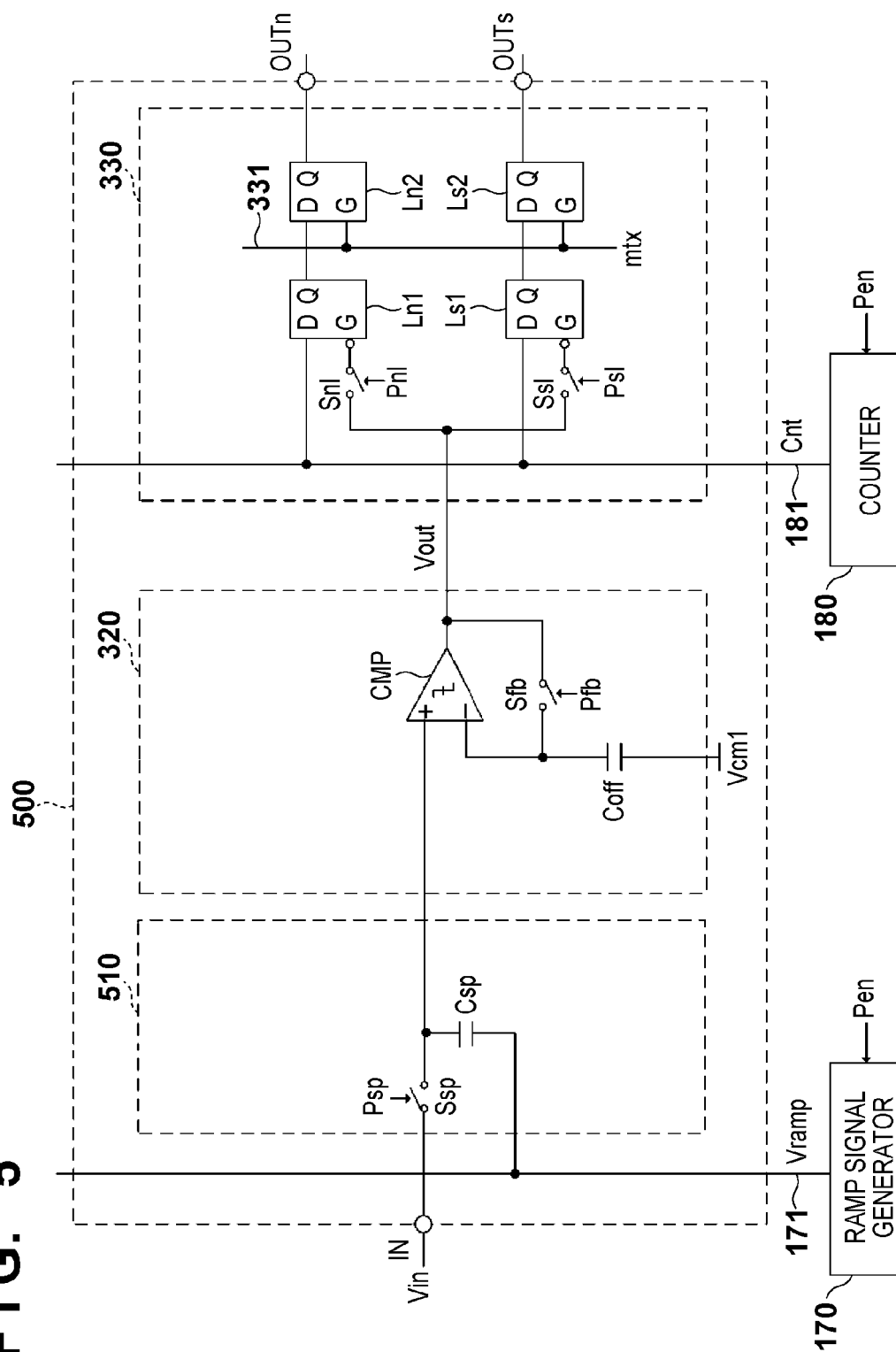
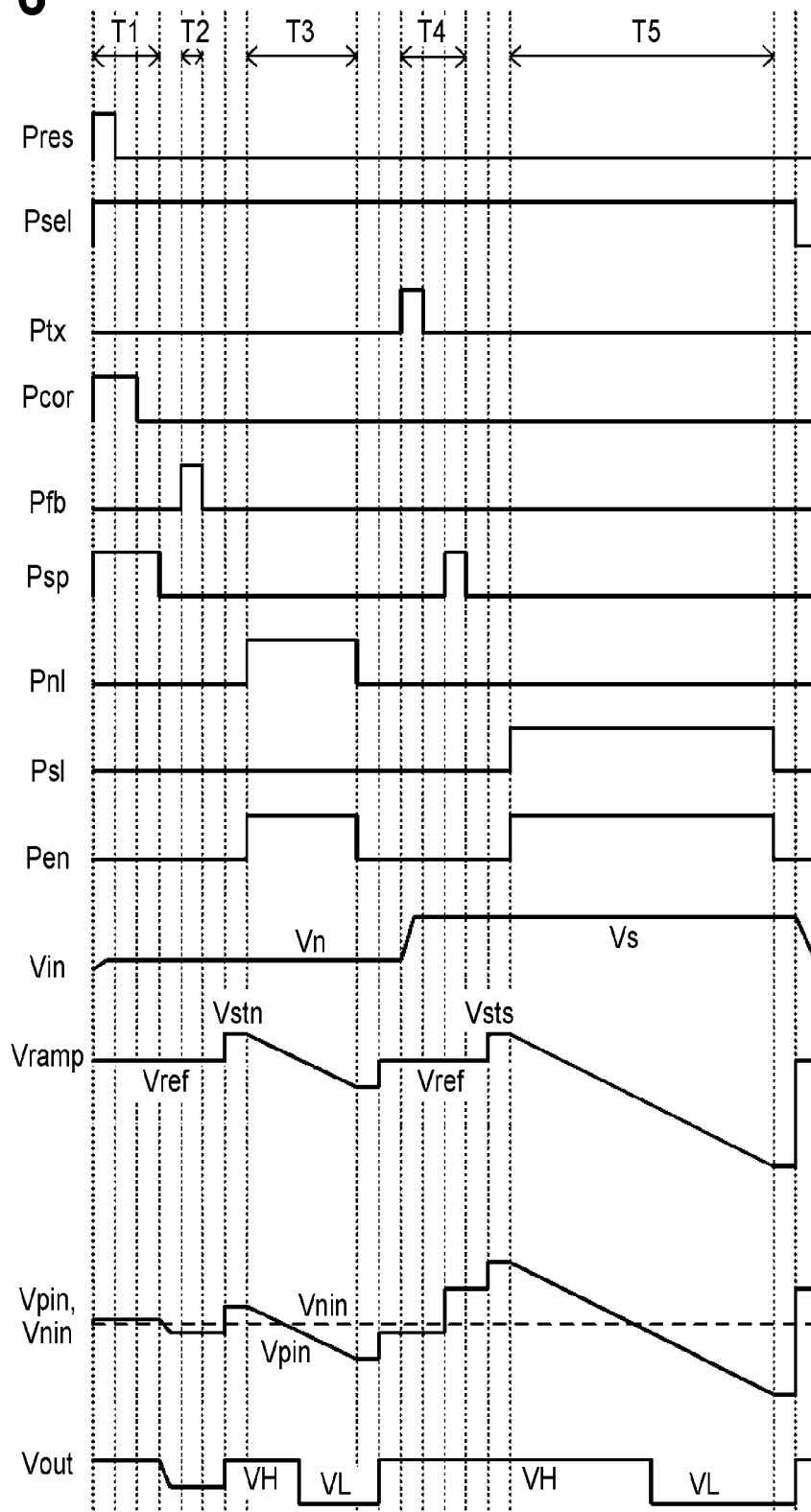


FIG. 6



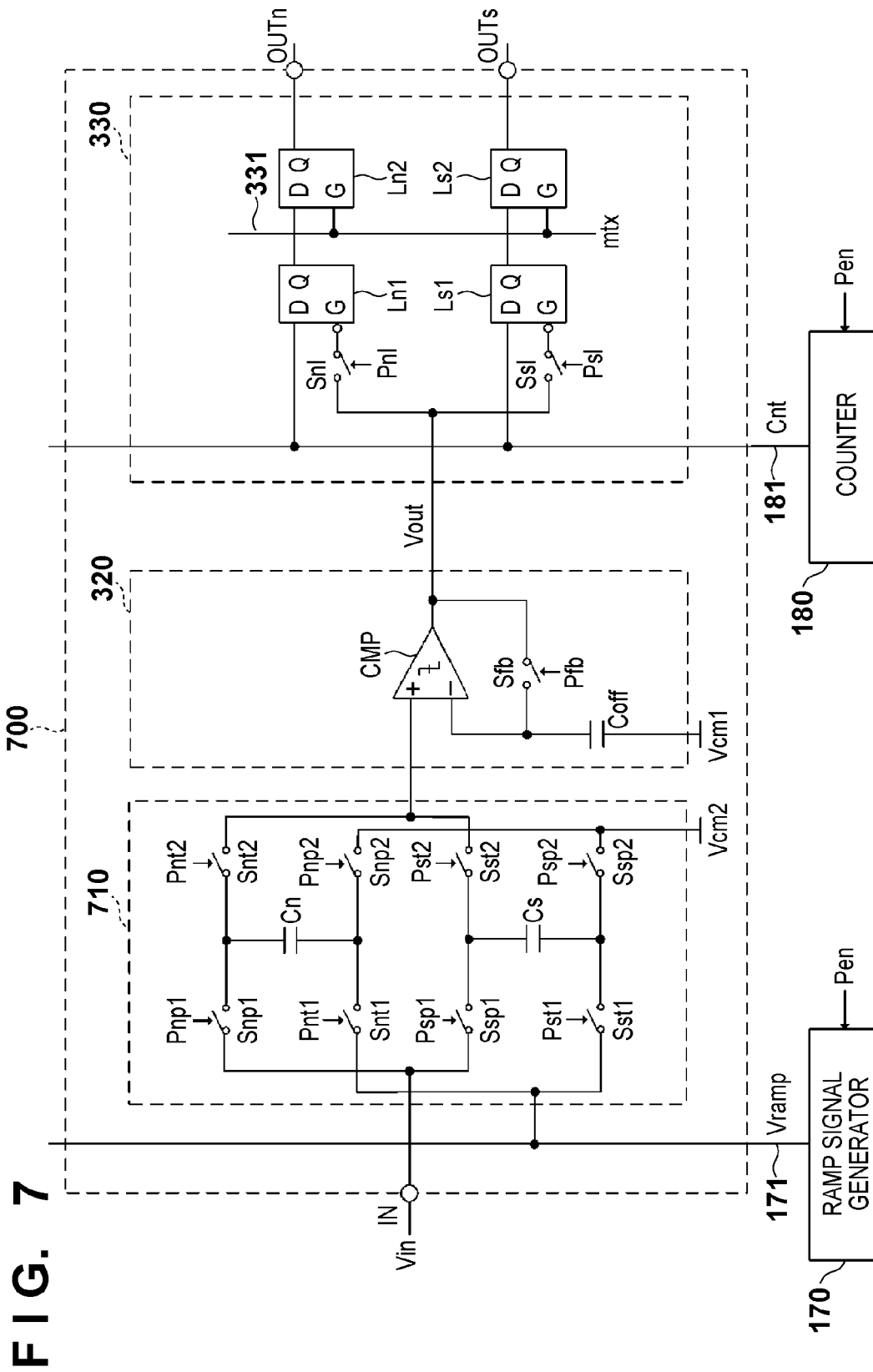
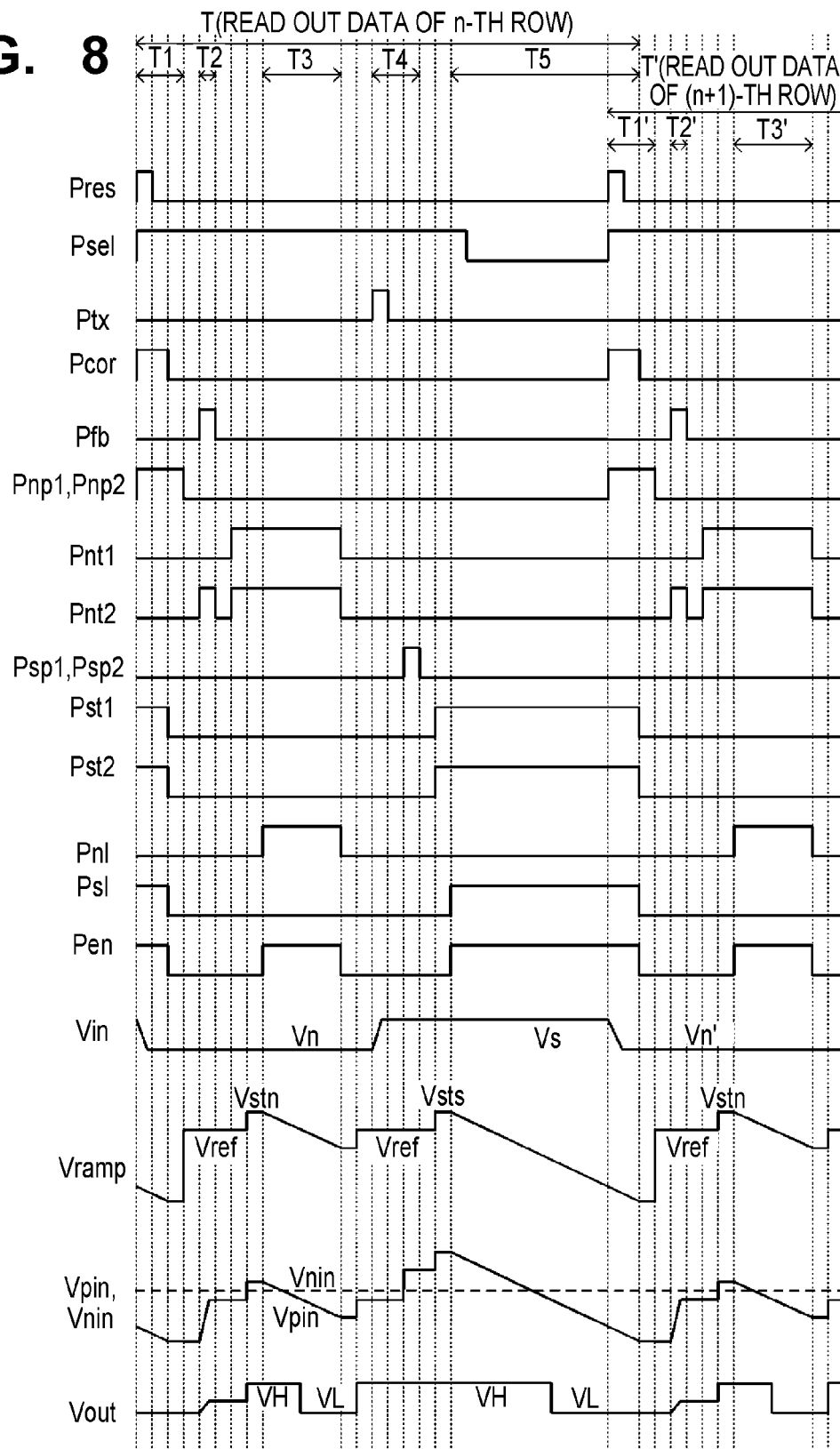


FIG. 8



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A/D CONVERTER AND SOLID-STATE IMAGING APPARATUS WITH OFFSET VOLTAGE CORRECTION

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an A/D converter and solid-state imaging apparatus.

2. Description of the Related Art

A technique which arranges A/D converters in correspondence with columns of pixels arranged in an array and converts signals from the respective pixels into digital data in a solid-state imaging apparatus is known. However, since offset voltages of comparators included in the respective A/D converters are different, an A/D conversion period has to be set in consideration of a maximum value of the offset voltages. U.S. Pat. No. 7,671,908 has proposed a technique for correcting an offset voltage by feeding back an output of the comparator included in each individual A/D converter to an input of that comparator.

SUMMARY OF THE INVENTION

The technique of U.S. Pat. No. 7,671,908 uses a controller to feed back the output of the comparator to its input. For this reason, the circuit arrangement of the A/D converter is complicated, and noise caused by the controller adversely influences the output of each comparator. Hence, an aspect of the present invention provides a technique for correcting an offset voltage of a comparator of each A/D converter by a simple arrangement.

An aspect of the present invention provides an A/D converter comprising: an input terminal for inputting an analog signal; a reference signal line for connecting to a signal source that generates a reference signal which changes temporally; a comparator which includes a non-inverting input terminal, an inverting input terminal, and an output terminal, and outputs, from the output terminal, an output signal according to a comparison result between a voltage supplied to the non-inverting input terminal and a voltage supplied to the inverting input terminal; a correction capacitor connected to the inverting input terminal of the comparator; and an output circuit which outputs digital data corresponding to the analog signal input to the input terminal, wherein in a first state in which a total charge of a first analog signal and an offset voltage of the comparator is held in the correction capacitor, a second analog signal input to the input terminal is supplied to the non-inverting input terminal of the comparator, and the second analog signal supplied to the non-inverting input terminal of the comparator or the total charge held in the correction capacitor is changed using the reference signal, thereby outputting, from the output circuit, digital data depending on a time from the beginning of the change until the output signal of the comparator changes as digital data corresponding to the second analog signal.

Further features of the present invention will become apparent from the following description of exemplary embodiments (with reference to the attached drawings).

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate embodiments of the invention, and together with the description, serve to explain the principles of the invention.

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FIG. 1 is a block diagram for explaining an example of the arrangement of a solid-state imaging apparatus 100 according to an embodiment of the present invention;

FIG. 2 is a circuit diagram for explaining an example of the arrangements of a pixel 111 and amplifier circuit 120 according to the embodiment of the present invention;

FIG. 3 is a circuit diagram for explaining an example of the arrangement of an A/D converter 300 according to the embodiment of the present invention;

FIG. 4 is a timing chart for explaining an example of the operation of the solid-state imaging apparatus 100 according to the embodiment of the present invention;

FIG. 5 is a circuit diagram for explaining an example of the arrangement of an A/D converter 500 according to the embodiment of the present invention;

FIG. 6 is a timing chart for explaining another example of the operation of the solid-state imaging apparatus 100 according to the embodiment of the present invention;

FIG. 7 is a circuit diagram for explaining an example of the arrangement of an A/D converter 700 according to the embodiment of the present invention; and

FIG. 8 is a timing chart for explaining still another example of the operation of the solid-state imaging apparatus 100 according to the embodiment of the present invention.

DESCRIPTION OF THE EMBODIMENTS

An embodiment of the present invention will be described hereinafter with reference to the accompanying drawings. The same reference numerals denote the same components throughout the drawings, and a repetitive description thereof will be avoided.

An example of a schematic arrangement of a solid-state imaging apparatus 100 according to one embodiment of the present invention will be described below with reference to FIG. 1. The solid-state imaging apparatus 100 is, for example, a CMOS image sensor, which photoelectrically converts incoming light indicating an object image, and externally outputs an electrical signal obtained by the photoelectric conversion as digital data. The solid-state imaging apparatus 100 can include an analog signal generator 110 including a pixel array formed by arranging a plurality of pixels 111 in a matrix. FIG. 1 illustrates four pixels 111 for the sake of simplicity, but the number of pixels 111 is not limited to this. Each pixel 111 photoelectrically converts incoming light to the solid-state imaging apparatus 100 into an analog signal.

The solid-state imaging apparatus 100 can further include a vertical scanning circuit 140. The vertical scanning circuit 140 supplies a driving pulse signal in turn to row selection lines 112 arranged in correspondence with respective pixel rows. When the driving pulse signal is supplied to each row selection line 112, analog signals are read out from respective pixels 111 included in the corresponding pixel row onto column signal lines 113. This embodiment will handle a case in which a reset-level signal of the pixel 111 and a signal obtained by superimposing a signal according to a charge generated by the photoelectric conversion on the reset-level signal are read out from the pixel 111. A difference between these signals represents an effective pixel value. The analog signal generator 110 outputs, based on these signals, a noise signal at a reset timing and a pixel signal depending on a charge obtained by the photoelectric conversion for each pixel 111.

The analog signal generator 110 can further include amplifier circuits 120 for respective column signal lines 113. Each amplifier circuit 120 amplifies the analog signal input from the corresponding pixel 111 via the column signal line 113,

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and supplies the amplified analog signal to a corresponding A/D converter 130. The solid-state imaging apparatus 100 can further include A/D converters 130 in correspondence with respective column signal lines 113. Each A/D converter converts the input analog signal into digital data, and outputs

The solid-state imaging apparatus 100 can further include a ramp signal generator 170 and counter 180. The ramp signal generator 170 generates a ramp signal V_{ramp} which changes in a slope pattern along with an elapse of time, and supplies the generated ramp signal V_{ramp} to the respective A/D converters 130 via a ramp signal line 171. As another embodiment, a signal source for generating another reference signal which changes temporally in place of the ramp signal may be used as the ramp signal generator 170. In this case, this reference signal is supplied to the respective A/D converters 130 via a reference signal supply line. The reference signal can use an arbitrary signal as long as it monotonically changes along with an elapse of time. An example of the reference signal includes a signal which changes step by step along with an elapse of time in addition to the aforementioned ramp signal. In this case, "monotonic change" means a change in potential without increasing in case of, for example, a monotonic decrease. The counter 180 supplies a count value C_{nt} to the respective A/D converters 130 via a count data line 181. As the counter 180, for example, a gray counter or binary counter may be used, and the counter 180 may have an up-down function. This embodiment will handle an example in which the plurality of A/D converters 130 share the ramp signal generator 170 and counter 180. Alternatively, each A/D converter 130 may have these components.

The solid-state imaging apparatus 100 can further include a horizontal scanning circuit 150 and signal processor 190. The horizontal scanning circuit 150 transfers digital data output from the A/D converters 130 onto a digital signal line 191 for respective columns. Digital data transferred onto the digital signal line 191 is supplied to the signal processor 190. In this embodiment, digital data corresponding to a noise signal and that corresponding to a pixel signal are read out in turn on the digital signal line 191. The signal processor 190 subtracts the digital data corresponding to the noise signal from that corresponding to the pixel signal, and externally outputs an effective pixel value.

The solid-state imaging apparatus 100 can further include a timing controller 195 which supplies pulse signals to the aforementioned components to control the operation of the solid-state imaging apparatus 100. FIG. 1 does not illustrate any signal lines used to transmit the pulse signals from the timing controller 195 to the respective components. The pulse signals supplied from the timing controller 195 will be described in detail later using timing charts to be described later.

In this embodiment, since the solid-state imaging apparatus 100 includes the amplifier circuits 120, the influences of noise components generated by the A/D converters 130 can be reduced. However, a modification of the solid-state imaging apparatus 100 may not include any amplifier circuit 120, and analog signals from the pixels 111 may be directly supplied to the A/D converters 130 via the column signal lines 113. Another modification of the solid-state imaging apparatus 100 may include CDS circuits in place of the amplifier circuits 120, and each CDS circuit may supply an analog signal obtained by subtracting a reset-level signal from a signal according to a charge generated by the pixel to the A/D converter 130. Each A/D converter converts this analog signal into digital data, and the horizontal scanning circuit 150 transfers the digital data corresponding to a pixel value of each

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pixel 111 to the signal processor 190. In the example shown in FIG. 1, the amplifier circuits 120, A/D converters 130, and horizontal scanning circuit 150 are arranged on one side of the pixel array. Alternatively, these components may be arranged on both the sides of the pixel array, and data may be distributed to the components on either one side for respective pixel columns.

An example of schematic arrangements of the pixel 111 and amplifier circuit 120 included in the solid-state imaging apparatus 100 will be described below with reference to the equivalent circuit diagram of FIG. 2. The pixel 111 and amplifier circuit 120 may have arbitrary arrangements as long as an analog signal required for calculating a pixel value of that pixel 111 can be supplied to the A/D converter 130. The pixel 111 includes a photodiode PD required to execute the photoelectric conversion and a plurality of transistors. The photodiode PD is connected to a floating diffusion FD via a transfer transistor T_{tx}. The floating diffusion FD is also connected to a voltage source VDD via a reset transistor T_{res}, and to a gate electrode of an amplifier transistor T_{amp}. A first main electrode of the amplifier transistor T_{amp} is connected to the voltage source VDD, and a second main electrode of the amplifier transistor T_{amp} is connected to the column signal line 113 via a selection transistor T_{sel}. A gate electrode of the selection transistor T_{sel} is connected to the row selection line 112. When the selection transistor T_{sel} is turned on, the amplifier transistor T_{amp} operates as a source-follower circuit together with a constant current source I_{cnst} inserted in the column signal line 113.

The amplifier circuit 120 includes illustrated circuit elements, and configures an inverting amplifier. A non-inverting input terminal of an amplifier AMP is connected to the column signal line 113 via a clamp capacitor C_o, and V_{cor} is supplied to an inverting input terminal of the amplifier AMP. An output terminal of the amplifier AMP is connected to the A/D converter 130. A parallel circuit of a feedback capacitor C_f and switch S_{cor} is connected between the non-inverting input terminal and output terminal of the amplifier AMP. By configuring a clamp circuit in this manner, the amplifier circuit 120 not only amplifies and outputs a signal input via the column signal line 113 by a ratio between the clamp capacitor C_o and feedback capacitor C_f, but also operates a CDS circuit. As a result, as a noise signal at a pixel reset timing, an offset of the amplifier circuit 120 is output from the analog signal generator 110. Also, as a pixel signal depending on a charge obtained by the photoelectric conversion, a signal from which a reset-level signal is removed is output from the analog signal generator 110. In an embodiment in which the amplifier circuit 120 is omitted, the analog signal generator 110 outputs a reset-level signal of the pixel as a noise signal, and a signal obtained by superimposing a signal according to a charge generated by the pixel on the reset-level signal as a pixel signal. In this embodiment, noise components generated as a result of resetting of the floating diffusion FD can be reduced.

A schematic arrangement of an A/D converter 300 as an example of the A/D converter 130 shown in FIG. 1 will be described below with reference to the equivalent circuit diagram shown in FIG. 3. The A/D converter 300 can include an input terminal IN, output terminals OUT_n and OUT_t, comparison circuit 320, and output circuit 330. To the input terminal IN, a noise signal and pixel signal for each pixel are input in turn as analog signals. The comparison circuit 320 executes comparison based on an analog signal input to the input terminal IN and the ramp signal V_{ramp} supplied from the ramp signal line 171, and outputs an output signal V_{out} of a level according to that comparison result. The output circuit

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330 outputs digital data based on the output signal V_{out} from the comparison circuit 320 and the count value Cnt supplied from the counter 180 from the output terminal OUT_n or OUT_s .

The comparison circuit 320 can include a comparator CMP, capacitor C_{off} , and switch S_{fb} . The capacitor C_{off} can function as a correction capacitor which corrects an offset of the comparator CMP. The comparator CMP can be a differential input comparator having a non-inverting input terminal and inverting input terminal. The non-inverting input terminal (“+” terminal in FIG. 3) of the comparator CMP is connected to the input terminal IN , and the inverting input terminal (“-” terminal in FIG. 3) of the comparator CMP is connected to a first electrode (upper electrode in FIG. 3) of the capacitor C_{off} . A second electrode (lower electrode in FIG. 3) of the capacitor C_{off} is connected to the ramp signal line 171. The switch S_{fb} connects the output terminal and inverting input terminal of the comparator CMP.

The output circuit 330 can include four latch circuits $Ln1$, $Ln2$, $Ls1$, and $Ls2$, which store digital data. Both of a D terminal of the latch circuit $Ln1$ and that of the latch circuit $Ls1$ are connected to the count data line 181. A G terminal of the latch circuit $Ln1$ is connected to the output line of the comparison circuit 320 via a switch S_{nl} , and a G terminal of the latch circuit $Ls1$ is connected to the output line of the comparison circuit 320 via a switch S_{sl} . A Q terminal of the latch circuit $Ln1$ is connected to a D terminal of the latch circuit $Ln2$, and a Q terminal of the latch circuit $Ls1$ is connected to a D terminal of the latch circuit $Ls2$. Both of a G terminal of the latch circuit $Ln2$ and that of the latch circuit $Ls2$ are connected to a signal line 331. A Q terminal of the latch circuit $Ln2$ is connected to the output terminal OUT_n , and a Q terminal of the latch circuit $Ls2$ is connected to the output terminal OUT_s . Since an inverting circuit is connected to the G terminals of the latch circuits $Ln1$ and $Ls1$, when the output from the comparison circuit 320 is at L level, data at the D terminals are output from the Q terminals.

An example of the operation of the solid-state imaging apparatus 100 having the A/D converters 300 will be described below with reference to the timing chart shown in FIG. 4. Respective pulse signals shown in FIG. 4 are generated by the timing controller 195, and are supplied to respective circuit elements in the solid-state imaging apparatus 100. That is, the timing controller 195 can control the operations of the respective components of the solid-state imaging apparatus 100. In FIG. 4, the operation of the pixel 111 of one row will be explained, but the same applies to the pixel 111 of another row. In FIG. 4, reference symbol V_{pin} denotes a voltage of the non-inverting input terminal of the comparator CMP; and V_{nin} , a voltage of the inverting input terminal of the comparator CMP. Operations of respective periods will be briefly explained. A noise signal V_n from the pixel 111 is supplied to the A/D converter 300 during a period T1, a charge of an offset voltage V_{off} of the comparator CMP is held in the capacitor C_{off} during a period T2, and the noise signal V_n is A/D-converted during a period T3. Subsequently, a pixel signal V_s from the pixel 111 is supplied to the A/D converter 300 during a period T4, and is A/D-converted during a period T5. The operations of the respective periods will be described in detail below.

At the beginning of the period T1, pulse signals $Pres$, $Psel$, and $Pcor$ respectively go H (High level), thus turning on the reset transistor T_{res} , selection transistor T_{sel} , and switch $Scor$. Thus, the floating diffusion FD is reset. In this state, the amplifier transistor T_{amp} operates as a source-follower, and a reset-level signal of the floating diffusion FD is read out onto the column signal line 113. When the pulse signal $Pcor$ goes

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L (Low level), the clamp capacitor C_o holds a potential difference between V_{cor} and the pixel output. The output of the amplifier circuit 120 at this time is supplied to the input terminal IN of the A/D converter 300 as the noise signal V_n (first analog signal). For this reason, the voltage V_{pin} of the non-inverting input terminal of the comparator CMP also becomes equal to V_n . The noise signal V_n contains an offset of the amplifier circuit 120. The noise signal V_n is continuously supplied until a pulse signal P_{tx} goes H.

At the beginning of the period T2, a pulse signal P_{fb} goes H, and the switch S_{fb} is turned on. As a result, the inverting input terminal and output terminal of the comparator CMP are short-circuited, and the comparator CMP operates as a voltage-follower. Since the voltage V_{pin} of the non-inverting input terminal of the comparator CMP is V_n , the voltage V_{out} of the output terminal is $V_n + V_{off}$, and the voltage V_{nin} of the inverting input terminal is also $V_n + V_{off}$. Also, the potential of the first electrode of the capacitor C_{off} is $V_n + V_{off}$. During the period T2, since the voltage of the ramp signal line 171 is V_{ref} , the potential of the second electrode of the capacitor C_{off} is V_{ref} . At the end of the period T2, the pulse signal P_{fb} goes L, the switch S_{fb} is turned off, and the capacitor C_{off} holds $V_n + V_{off} - V_{ref}$ as a voltage across its two electrodes. Then, the A/D converter 130 is set in a ready state (that can correspond to a first state).

During an interval between the periods T2 and T3, the ramp signal generator 170 changes a voltage to be supplied onto the ramp signal line 171 to V_{stn} in accordance with a pulse signal (not shown) from the timing controller 195. As a result, the potential of the second electrode of the capacitor C_{off} becomes V_{stn} , and the potential of the first electrode of the capacitor C_{off} becomes $V_n + V_{off} - V_{ref} + V_{stn}$ accordingly. Since V_{stn} is set to be a sufficiently small value, the voltage V_{nin} of the inverting input terminal of the comparator CMP is lower than the voltage V_{pin} of the non-inverting input terminal at the beginning of the period T3. More specifically, V_{stn} is set to meet $V_{nin} - V_{pin} < V_{off}$. As a result, at the beginning of the period T3, the output signal V_{out} of the comparator CMP becomes V_H . At the beginning of the period T3, a pulse signal P_{en} goes H, the ramp signal generator 170 begins to change the ramp signal V_{ramp} to be supplied onto the ramp signal line 171, and the counter 180 begins to count and supplies the count value Cnt onto the count data line 181. In this embodiment, when the pulse signal P_{en} goes H, the ramp signal generator 170 supplies the ramp signal V_{ramp} which begins from V_{stn} and increases linearly along with an elapse of time onto the ramp signal line 171. Furthermore, when a pulse signal P_{nl} goes H, the switch S_{nl} is turned on. As a result, the output terminal of the comparator CMP and the G terminal of the latch circuit $Ln1$ are connected.

When the ramp signal V_{ramp} begins to increase, the potential of the second electrode of the capacitor C_{off} increases, and that of the first electrode of the capacitor C_{off} increases accordingly. Then, when the voltage V_{nin} of the inverting input terminal of the comparator CMP becomes equal to $V_n + V_{off}$, the output signal V_{out} from the comparator CMP changes from V_H to V_L . As a result, an L-level signal is supplied to the G terminal of the latch circuit $Ln1$, and the count value Cnt supplied to the D terminal at that time is stored in the latch circuit $Ln1$ and is output from the Q terminal. The output signal V_{out} of the comparator CMP is inverted when the voltage V_{nin} of the non-inverting input terminal of the comparator CMP becomes equal to $V_n + V_{off}$. For this reason, the latch circuit $Ln1$ stores a count value corresponding to a time required for the voltage of the non-inverting input terminal of the comparator CMP to change from $V_n + V_{off} - V_{ref} + V_{stn}$ to $V_n + V_{off}$, that is, a count value

corresponding to $V_{ref}-V_{stn}$. The count value stored in the latch circuit Ln1 is digital data when the noise signal Vn as the analog signal is converted.

At the beginning of the period T4, the pulse signal Ptx goes H, and the transfer transistor Ttx is turned on. Then, a charge accumulated on the photodiode PD is transferred to the floating diffusion FD. In this state, the amplifier transistor Tamp operates as a source-follower, and a signal obtained by superimposing a signal according to the charge accumulated on the photodiode PD on the reset-level signal of the floating diffusion FD is read out onto the column signal line 113. The readout signal is amplified by the amplifier circuit 120, and is supplied to the input terminal IN of the A/D converter 300 as a pixel signal Vs (second analog signal). For this reason, the voltage Vpin of the non-inverting input terminal of the comparator CMP also becomes Vs. Since the clamp capacitor Co holds a potential difference between the pixel output during the period T1 and Vcor, the signal output from the amplifier circuit 120 ideally does not include any noise component generated upon resetting of the floating diffusion FD.

During an interval between the periods T4 and T5, the ramp signal generator 170 changes a voltage to be supplied onto the ramp signal line 171 to Vsts in accordance with a pulse signal (not shown) from the timing controller 195. As a result, the potential of the second electrode of the capacitor Coff becomes Vsts, and that of the first electrode of the capacitor Coff becomes $V_n+V_{off}-V_{ref}+V_{sts}$ accordingly. Since Vsts is set to be a sufficiently small value, the voltage Vnin of the inverting input terminal of the comparator CMP is lower than the voltage Vpin of the non-inverting input terminal at the beginning of the period T5. More specifically, Vsts is set to meet $V_{nin}-V_{pin}<V_{off}$. As a result, at the beginning of the period T5, the output signal Vout of the comparator CMP becomes VH. At the beginning of the period T5, the pulse signal Pen goes H, the ramp signal generator 170 begins to change the ramp signal Vram to be supplied onto the ramp signal line 171, and the counter 180 begins to count and supplies the count value Cnt onto the count data line 181. In this embodiment, when the pulse signal Pen goes H, the ramp signal generator 170 supplies the ramp signal Vram which begins from Vsts and increases linearly along with an elapse of time onto the ramp signal line 171. Furthermore, when a pulse signal Psl goes H, the switch Ssl is turned on. As a result, the output terminal of the comparator CMP and the G terminal of the latch circuit Ls1 are connected.

When the ramp signal Vram begins to increase, the potential of the second electrode of the capacitor Coff increases, and that of the first electrode of the capacitor Coff increases accordingly. Then, when the voltage Vnin of the inverting input terminal of the comparator CMP becomes equal to V_s+V_{off} , the output signal Vout from the comparator CMP changes from VH to VL. As a result, an L-level signal is supplied to the G terminal of the latch circuit Ls1, and the count value Cnt supplied to the D terminal at that time is stored in the latch circuit Ls1 and is output from the Q terminal. The output signal Vout of the comparator CMP is inverted when the voltage Vnin of the non-inverting input terminal of the comparator CMP becomes equal to V_s+V_{off} . For this reason, the latch circuit Ls1 stores a count value corresponding to a time required for the voltage of the non-inverting input terminal of the comparator CMP to change from $V_n+V_{off}-V_{ref}+V_{sts}$ to V_s+V_{off} , that is, a count value corresponding to $V_s-V_n+V_{ref}-V_{sts}$. The count value stored in the latch circuit Ls1 is digital data when the pixel signal Vs as the analog signal is converted.

After the period T5, a pulse signal mtX (not shown in FIG. 4) is supplied to the G terminals of the latch circuit Ln2 and

Ls2. Then, the latch circuit Ln2 stores the output of the latch circuit Ln1 and outputs it from the output terminal OUTn. Also, the latch circuit Ls2 stores the output of the latch circuit Ls1 and outputs it from the output terminal OUTs. Then, the horizontal scanning circuit 150 reads out digital data output from the output terminals OUTn and OUTs in turn onto the digital signal line 191. The signal processor 190 calculates a difference between the digital data which represents $V_s-V_n+V_{ref}-V_{sts}$ and that which represents $V_{ref}-V_{stn}$. With this calculation, digital data which represents $V_s-V_n+V_{stn}-V_{sts}$ is obtained. By setting $V_{stn}=V_{sts}$, the signal processor 190 can acquire digital data corresponding to V_s-V_n . Alternatively, by adjusting Vstn and Vsts, an offset may be given to the digital data to be acquired by the signal processor 190.

According to the aforementioned embodiment, since a total charge of the noise signal Vn and offset voltage Voff of the comparator CMP is held in the capacitor Coff to correct the offset voltage, the circuit arrangement can be simplified. Since there is no influence of the offset voltage Voff during the A/D conversion period T3 of the noise signal Vn and the A/D conversion period T5 of the pixel signal Vs, variations of offset voltages among the A/D converters 130, which are arranged in correspondence with the respective pixel columns, need not be considered. For this reason, the A/D conversion periods T3 and T5 of the noise signal Vn and pixel signal Vs can be shortened, thus improving the frame rate and A/D conversion precision of the solid-state imaging apparatus 100. Furthermore, since the influence of the noise signal Vn can also be eliminated during the A/D conversion period of the noise signal Vn, the A/D conversion period T3 of the noise signal Vn can be further shortened.

A schematic arrangement of an A/D converter 500 as another example of the A/D converter 130 shown in FIG. 1 will be described below with reference to the equivalent circuit diagram of FIG. 5. The same reference numerals in FIG. 5 denote components common to the A/D converter 300 shown in FIG. 3, and a repetitive description thereof will be avoided. The A/D converter 500 can include an input terminal IN, output terminals OUTn and OUTs, holding circuit 510, comparison circuit 320, and output circuit 330. The holding circuit 510 samples and holds an analog signal Vin input to the input terminal IN. The comparison circuit 320 executes comparison based on the analog signal held in the holding circuit 510 and the ramp signal Vram supplied from the ramp signal line 171, and outputs an output signal Vout of a level according to that comparison result.

The holding circuit 510 can include a capacitor Csp and switch Ssp. The capacitor Csp can function as a sampling capacitor which samples a noise signal Vn and pixel signal Vs. The switch Ssp connects the input terminal IN and comparison circuit 320. A first electrode (upper electrode in FIG. 5) of the capacitor Csp is connected to the comparison circuit 320, and a second electrode (lower electrode in FIG. 5) of the capacitor Csp is connected to the ramp signal line 171.

Unlike in the A/D converter 300 shown in FIG. 3, in the A/D converter 500, the non-inverting input terminal of the comparator CMP of the comparison circuit 320 is connected to the holding circuit 510, and the second electrode (lower electrode in FIG. 5) of the capacitor Coff is connected to a voltage source Vcm1.

An example of the operation of the solid-state imaging apparatus 100 having the A/D converters 500 will be described below with reference to the timing chart shown in FIG. 6. Respective pulse signals shown in FIG. 6 are generated by the timing controller 195, and are supplied to respective circuit elements in the solid-state imaging apparatus 100. In FIG. 6, the operation of the pixel 111 of one row will be

explained, but the same applies to the pixel 111 of another row. In FIG. 6, reference symbol V_{pin} denotes a voltage of the non-inverting input terminal of the comparator CMP; and V_{nin} , a voltage of the inverting input terminal of the comparator CMP. Periods T1 to T5 in the timing chart of FIG. 6 correspond to the periods T1 to T5 in the timing chart of FIG. 4. The operations of the respective periods will be described in detail below.

During the period T1, as in the period T1 in the timing chart of FIG. 4, a noise signal V_n is supplied to the input terminal IN of the A/D converter 500. The noise signal V_n is continuously supplied until a pulse signal P_{tx} goes H. At the beginning of the period T1, a pulse signal P_{sp} goes H, and the switch S_{sp} is turned on. As a result, the input terminal IN is connected to the non-inverting input terminal of the comparator CMP, and the voltage V_{pin} of the non-inverting terminal becomes V_n . Also, the potential of the first electrode of the capacitor C_{sp} becomes V_n . Since the voltage of the ramp signal line 171 is V_{ref} during period T1, the potential of the second electrode of the capacitor C_{sp} becomes V_{ref} . At the end of the period T1, the pulse signal P_{sp} goes L to turn off the switch S_{sp} , and the capacitor C_{sp} holds $V_n - V_{ref}$ as a voltage across its two electrodes.

At the beginning of the period T2, a pulse signal P_{fb} goes H, and the switch S_{fb} is turned on. As a result, the inverting input terminal and output terminal of the comparator CMP are short-circuited, and the comparator CMP operates as a voltage-follower. Since the voltage V_{pin} of the non-inverting input terminal of the comparator CMP is V_n , the voltage V_{out} of the output terminal is $V_n + V_{off}$, and the voltage V_{nin} of the inverting input terminal is also $V_n + V_{off}$. Also, the potential of the first electrode of the capacitor C_{off} is $V_n + V_{off}$. The potential of the second electrode of the capacitor C_{off} is fixed at V_{cm1} . At the end of the period T2, the pulse signal P_{fb} goes L to turn off the switch S_{fb} , and the capacitor C_{off} holds $V_n + V_{off} - V_{cm1}$ as a voltage across its two electrodes. The voltage V_{nin} of the inverting input terminal of the comparator CMP is maintained at $V_n + V_{off}$ until the period T5 ends.

During an interval between the periods T2 and T3, the ramp signal generator 170 changes a voltage to be supplied onto the ramp signal line 171 to V_{stn} in accordance with a pulse signal (not shown) from the timing controller 195. As a result, the potential of the second electrode of the capacitor C_{sp} becomes V_{stn} , and that of the first electrode of the capacitor C_{sp} becomes $V_n - V_{ref} + V_{stn}$ accordingly. Since V_{stn} is set to be a sufficiently large value, the voltage V_{nin} of the inverting input terminal of the comparator is lower than the voltage V_{pin} of the non-inverting input terminal at the beginning of the period T3. More specifically, V_{stn} is set to meet $V_{nin} - V_{pin} < V_{off}$. As a result, at the beginning of the period T3, the output signal V_{out} of the comparator CMP becomes VH. At the beginning of the period T3, a pulse signal P_{en} goes H, the ramp signal generator 170 begins to change the ramp signal V_{ramp} to be supplied onto the ramp signal line 171, and the counter 180 begins to count and supplies the count value C_{nt} onto the count data line 181. In this embodiment, when the pulse signal P_{en} goes H, the ramp signal generator 170 supplies the ramp signal V_{ramp} which begins from V_{stn} and decreases linearly along with an elapse of time onto the ramp signal line 171. Furthermore, when a pulse signal P_{nl} goes H, the switch S_{nl} is also turned on. As a result, the output terminal of the comparator CMP and the G terminal of the latch circuit Ln1 are connected.

When the ramp signal V_{ramp} begins to decrease, the potential of the second electrode of the capacitor C_{sp} decreases, and that of the first electrode of the capacitor C_{sp} decreases accordingly. When the voltage V_{pin} of the non-inverting

input terminal of the comparator CMP becomes equal to V_n , the output signal V_{out} from the comparator CMP changes from VH to VL. As a result, an L-level signal is supplied to the G terminal of the latch circuit Ln1, and the count value C_{nt} supplied to the D terminal at that time is stored in the latch circuit Ln1 and is output from the Q terminal. The output signal V_{out} of the comparator CMP is inverted when the voltage V_{pin} of the non-inverting input terminal of the comparator CMP becomes equal to V_n . For this reason, the latch circuit Ln1 stores a count value corresponding to a time required for the voltage of the non-inverting input terminal of the comparator CMP to change from $V_n - V_{ref} + V_{stn}$ to V_n , that is, a count value corresponding to $V_{ref} - V_{stn}$. The count value stored in the latch circuit Ln1 is digital data when the noise signal V_n as the analog signal is converted. After the end of the period T3, the ramp signal generator 170 returns the voltage of the ramp signal line 171 to V_{ref} .

At the beginning of the period T4, a pulse signal P_{tx} goes H, and a pixel signal V_s is supplied to the input terminal IN of the A/D converter 500 in the same manner as in the description of the timing chart shown in FIG. 4. In the middle of the period T4, the pulse signal P_{sp} goes H, and the switch S_{sp} is turned on. As a result, the input terminal IN and the non-inverting input terminal of the comparator CMP are connected, and the voltage V_{pin} of the non-inverting input terminal becomes V_s . Also, the potential of the first electrode of the capacitor C_{sp} becomes V_s . Since the voltage of the ramp signal line 171 is V_{ref} during the period T4, the potential of the second electrode of the capacitor C_{sp} becomes V_{ref} . In the middle of the period T4, the pulse signal P_{sp} goes L to turn off the switch S_{sp} , and the capacitor C_{sp} holds $V_s - V_{ref}$ as a voltage across its two electrodes.

During an interval between the periods T4 and T5, the ramp signal generator 170 changes a voltage to be supplied onto the ramp signal line 171 to V_{sts} in accordance with a pulse signal (not shown) from the timing controller 195. As a result, the potential of the second electrode of the capacitor C_{sp} becomes V_{sts} , and that of the first electrode of the capacitor C_{sp} becomes $V_s - V_{ref} + V_{sts}$ accordingly. Since V_{sts} is set to be a sufficiently large value, the voltage V_{nin} of the inverting input terminal of the comparator CMP is lower than the voltage V_{pin} of the non-inverting input terminal at the beginning of the period T5. More specifically, V_{sts} is set to meet $V_{nin} - V_{pin} < V_{off}$. As a result, at the beginning of the period T5, the output signal V_{out} of the comparator CMP becomes VH. At the beginning of the period T5, the pulse signal P_{en} goes H, the ramp signal generator 170 begins to change the ramp signal V_{ramp} to be supplied onto the ramp signal line 171, and the counter 180 begins to count and supplies the count value C_{nt} onto the count data line 181. In this embodiment, when the pulse signal P_{en} goes H, the ramp signal generator 170 supplies the ramp signal V_{ramp} which begins from V_{sts} and decreases linearly along with an elapse of time onto the ramp signal line 171. Furthermore, when the pulse signal P_{sl} goes H, the switch S_{sl} is turned on. As a result, the output terminal of the comparator CMP and the G terminal of the latch circuit Ls1 are connected.

When the ramp signal V_{ramp} begins to decrease, the potential of the second electrode of the capacitor C_{sp} decreases, and that of the first electrode of the capacitor C_{sp} decreases accordingly. Then, when the voltage V_{pin} of the non-inverting input terminal of the comparator CMP becomes equal to V_n , the output signal V_{out} from the comparator CMP changes from VH to VL. As a result, an L-level signal is supplied to the G terminal of the latch circuit Ls1, and the count value C_{nt} supplied to the D terminal at that time is stored in the latch circuit Ls1 and is output from the Q terminal. The output

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signal V_{out} of the comparator CMP is inverted when the voltage V_{nin} of the non-inverting input terminal of the comparator CMP becomes equal to V_n . For this reason, the latch circuit Ls1 stores a count value corresponding to a time required for the voltage of the non-inverting input terminal of the comparator CMP to change from $V_s - V_{ref} + V_{sts}$ to V_n , that is, a count value corresponding to $V_n - V_s + V_{ref} - V_{sts}$. The count value stored in the latch circuit Ls1 is digital data when the pixel signal V_s as the analog signal is converted.

After the period T5, as in the description of the timing chart of FIG. 4, the signal processor 190 calculates a difference between digital data which represents $V_n - V_s + V_{ref} - V_{sts}$ and that which represents $V_{ref} - V_{stn}$. With this calculation, digital data which represents $V_n - V_s + V_{stn} - V_{sts}$ is obtained. By setting $V_{stn} = V_{sts}$, the signal processor 190 can acquire digital data corresponding to $V_s - V_n$. Alternatively, by adjusting V_{stn} and V_{sts} , an offset may be given to the digital data to be acquired by the signal processor 190. When the solid-state imaging apparatus 100 includes the A/D converter 500 shown in FIG. 5, the same effects as those obtained when the solid-state imaging apparatus 100 includes the A/D converter 300 shown in FIG. 3 can be obtained.

A schematic arrangement of an A/D converter 700 as still another example of the A/D converter 130 shown in FIG. 1 will be described below with reference to the equivalent circuit diagram of FIG. 7. The same reference numerals in FIG. 7 denote components common to the A/D converter 500 shown in FIG. 5, and a repetitive description thereof will be avoided. The A/D converter 700 can include an input terminal IN, output terminals OUTn and OUTs, holding circuit 710, comparison circuit 320, and output circuit 330. The holding circuit 710 samples and holds an analog signal V_{in} input to the input terminal IN. The comparison circuit 320 executes comparison based on the analog signal held in the holding circuit 710 and the ramp signal V_{ramp} supplied from the ramp signal line 171, and outputs an output signal V_{out} of a level according to that comparison result. The connection relationship of the comparison circuit 320 is the same as that in the A/D converter 500 shown in FIG. 5.

Unlike in the holding circuit 510 shown in FIG. 5, the holding circuit 710 can include two capacitors, that is, capacitors C_n and C_s , and one or more switches used to switch connection destinations of these capacitors C_n and C_s . A first electrode (upper electrode in FIG. 7) of one capacitor C_n is connected to the input terminal IN via a switch Snp1 and to the comparison circuit 320 via a switch Snt2. A second electrode (lower electrode in FIG. 7) of the capacitor C_n is connected to a voltage source V_{cm2} via a switch Snp2 and to the ramp signal line 171 via a switch Snt1. Likewise, a first electrode (upper electrode in FIG. 7) of the other capacitor C_s is connected to the input terminal IN via a switch Ssp1 and to the comparison circuit 320 via a switch Sst2. A second electrode (lower electrode in FIG. 7) of the capacitor C_s is connected to the voltage source V_{cm2} via a switch Ssp2 and to the ramp signal line 171 via a switch Sst1. A voltage to be supplied from the voltage source V_{cm2} may or may not be equal to V_{ref} or V_{cm1} .

An example of the operation of the solid-state imaging apparatus 100 having the A/D converters 700 will be described below with reference to the timing chart shown in FIG. 8. Respective pulse signals shown in FIG. 8 are generated by the timing controller 195, and are supplied to respective circuit elements in the solid-state imaging apparatus 100. FIG. 8 will explain the operations of the pixel 111 (first pixel) of the n-th row and the pixel 111 (second pixel) of the (n+1)-th row, from which data are continuously read out. Digital data of the pixel 111 of the n-th row is read out to the signal

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processor 190 during a period T, and digital data of the pixel 111 of the (n+1)-th row is read out to the signal processor 190 during a period T'. Since the operations in the periods T and T' are the same, only a former half of the period T' is shown. Since the periods T and T' partially overlap each other, a time required for the A/D conversion can be shortened. In FIG. 8, reference symbol V_{pin} denotes a voltage of the non-inverting input terminal of the comparator CMP; and V_{nin} , a voltage of the inverting input terminal of the comparator CMP. Periods T1 to T5 in the timing chart of FIG. 8 correspond to the periods T1 to T5 in the timing chart of FIG. 6. The operations of the respective periods will be described in detail below. Since periods T1' to T3' for the pixel 111 of the (n+1)-th row are the same as periods T1 to T3 for the pixel of the n-th row, a description thereof will not be repeated.

During the period T1, as in the timing chart shown in FIG. 6, a noise signal V_n is input to the input terminal IN of the A/D converter 700. Also, at the beginning of the period T1, pulse signals Pnp1 and Pnp2 go H, and the switches Snp1 and Snp2 are turned on. As a result, the input terminal IN and voltage source V_{cm2} are connected via the capacitor C_n , and the capacitor C_n holds a difference between V_{cm2} and the noise signal V_n . More specifically, the potential of the first electrode of the capacitor C_n becomes equal to V_n , and that of the second electrode of the capacitor C_n becomes equal to V_{cm2} . After the end of the period T1, the pulse signals Pnp1 and Pnp2 go L, and the switches Snp1 and Snp2 are turned off.

At the beginning of the period T2, pulse signals Pfb and Pnt2 go H, and the switches Sfb and Pnt2 are turned on. As a result, the first electrode of the capacitor C_n is connected to the non-inverting input terminal of the comparator. Also, the inverting input terminal and output terminal of the comparator CMP are short-circuited, and the comparator CMP operates as a voltage-follower. Since the voltage V_{pin} of the non-inverting input terminal of the comparator CMP is V_n , the voltage V_{out} of the output terminal becomes $V_n + V_{off}$, and the voltage V_{nin} of the inverting input terminal also becomes $V_n + V_{off}$. The potential of the first electrode of the capacitor C_{off} becomes $V_n + V_{off}$. The potential of the second electrode of the capacitor C_{off} is fixed at V_{cm1} . At the end of the period T2, the pulse signal Pfb goes L to turn off the switch Sfb, and the capacitor C_{off} holds $V_n + V_{off} - V_{cm1}$ as a voltage across its two electrodes. The voltage V_{nin} of the inverting input terminal of the comparator CMP is maintained at $V_n + V_{off}$ until the period T5 ends.

Next, during the period T3, the noise signal V_n is A/D-converted. During the period T3, pulse signals Pnt1 and Pnt2 go H, and the switches Snt1 and Snt2 are turned on. As a result, the non-inverting input terminal of the comparator CMP and the ramp signal line 171 are connected via the capacitor C_n . In the same manner as in the timing chart of FIG. 6, the noise signal V_n is A/D-converted.

Next, at the beginning of the period T4, a pulse signal Ptx goes H, and a pixel signal V_s is supplied to the input terminal IN of the A/D converter 700 as in the timing chart of FIG. 6. After that, in the middle of the period T4, pulse signals Psp1 and Psp2 go H, and the switches Ssp1 and Ssp2 are turned on. As a result, the input terminal IN and voltage source V_{cm2} are connected via the capacitor C_s , and the capacitor C_s holds a difference between V_{cm2} and the pixel signal V_s . More specifically, the potential of the first electrode of the capacitor C_s becomes equal to the pixel signal V_s , and that of the second electrode of the capacitor C_s becomes equal to V_{cm2} . After the end of the period T4, the pulse signals Psp1 and Psp2 go L, and the switches Ssp1 and Ssp2 are turned off.

Next, during the period T5, the pixel signal V_s is A/D-converted. During the period T5, pulse signals Pst1 and Pst2

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go H, and the switches Pst1 and Pst2 are turned on. As a result, the non-inverting input terminal of the comparator CMP and ramp signal line 171 are connected via the capacitor Cs, and the pixel signal is A/D-converted as in the timing chart shown in FIG. 6.

When the solid-state imaging apparatus 100 has the A/D converter 700 shown in FIG. 7, the same effects as those obtained when the solid-state imaging apparatus 100 has the A/D converter 300 shown in FIG. 3 can be obtained. As shown in the timing chart of FIG. 8, in this embodiment, the A/D conversion period T5 of the pixel signal Vs of the pixel 111 of the n-th row overlaps a holding period T1' of a noise signal Vn' of the pixel 111 of the (n+1)-th row. Thus, the overall A/D conversion period required for the pixels 111 of the solid-state imaging apparatus 100 can be shortened. Also, by controlling the A/D converter 700 so as not to simultaneously connect the capacitors Cn and Cs to a common circuit arrangement, crosstalk via a common impedance can be reduced. Since Vcm2 is supplied to the capacitor Cs while the ramp signal Vram is supplied to the capacitor Cn, crosstalk due to capacitive coupling can also be reduced. Therefore, the solid-state imaging apparatus 100 having the A/D converters 700 can attain imaging operations at a high frame rate in which interlinear crosstalk can be eliminated.

While the present invention has been described with reference to exemplary embodiments, it is to be understood that the invention is not limited to the disclosed exemplary embodiments. The scope of the following claims is to be accorded the broadest interpretation so as to encompass all such modifications and equivalent structures and functions.

This application claims the benefit of Japanese Patent Application No. 2011-202335, filed Sep. 15, 2011, which is hereby incorporated by reference herein in its entirety.

What is claimed is:

1. An A/D converter comprising:
an input terminal for inputting an analog signal;
a reference signal line for connecting to a signal source that generates a reference signal which changes temporally;
a comparator which includes a non-inverting input terminal, an inverting input terminal, and an output terminal, and outputs, from the output terminal, an output signal according to a comparison result between a voltage supplied to the non-inverting input terminal and a voltage supplied to the inverting input terminal;
a correction capacitor connected to the inverting input terminal of said comparator; and
an output circuit which outputs digital data corresponding to the analog signal input to said input terminal,
wherein in a first state in which a total charge of a first analog signal and an offset voltage of said comparator is held in said correction capacitor, a second analog signal input to said input terminal is supplied to the non-inverting input terminal of said comparator, and the second analog signal supplied to the non-inverting input terminal of said comparator or the total voltage held in said correction capacitor is changed using the reference signal, thereby outputting, from said output circuit, digital data depending on a time from the beginning of the change until the output signal of said comparator changes as digital data corresponding to the second analog signal.

2. The A/D converter according to claim 1, wherein in the first state, the first analog signal is supplied to the non-inverting input terminal of said comparator, and the first analog signal supplied to the non-inverting input terminal of said comparator or the total charge held in said correction capacitor is changed using the reference signal, thereby further

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outputting, from said output circuit, digital data depending on a time from the beginning of the change until the output signal of said comparator changes as digital data corresponding to the first analog signal.

3. The A/D converter according to claim 1, further comprising:

a switch which connects the inverting input terminal and the output terminal of said comparator,
wherein the first analog signal is supplied to the non-inverting input terminal of said comparator in a state in which said switch is ON, and said switch is turned off after the total voltage is held in said correction capacitor, thereby setting the first state.

4. The A/D converter according to claim 1, wherein the reference signal is a ramp signal.

5. The A/D converter according to claim 1, wherein said correction capacitor includes a first electrode and a second electrode,

the first electrode of said correction capacitor is connected to the inverting input terminal of said comparator, and the reference signal is supplied to the second electrode of said correction capacitor in the first state, thereby changing the total charge held in said correction capacitor.

6. The A/D converter according to claim 1, further comprising:

a sampling capacitor which includes a first electrode connected to the non-inverting input terminal of said comparator, and a second electrode,

wherein in the first state in which the second analog signal is further held in said sampling capacitor, the reference signal is supplied to the second electrode of said sampling capacitor, thereby changing the second analog signal supplied to the non-inverting input terminal of said comparator.

7. The A/D converter according to claim 6, wherein said A/D converter comprises two sampling capacitors equivalent to said sampling capacitor, and

one sampling capacitor holds the first analog signal, and the other sampling capacitor holds the second analog signal.

8. A solid-state imaging apparatus comprising:

an A/D converter of claim 1;

an analog signal generator which has a plurality of pixels, and generates pixel signals depending on charges obtained by photoelectric conversion for respective pixels; and

a controller which supplies the pixel signal to said A/D converter as the second analog signal, and controls said A/D converter to output digital data corresponding to the pixel signal.

9. The apparatus according to claim 8, wherein each of the plurality of pixels further generates a noise signal at a pixel reset timing, and

said controller supplies the noise signal to said A/D converter as the first analog signal.

10. The apparatus according to claim 8, wherein said analog signal generator further comprises an amplifier circuit which amplifies a signal from the pixel, and

said amplifier circuit generates the noise signal based on a reset-level signal of the pixel supplied from the plurality of pixels, and generates the pixel signal based on a signal obtained by superimposing a signal according to a charge generated by photoelectric conversion on the reset-level signal.

11. The apparatus according to claim 8, wherein said A/D converter is arranged for each pixel column of the pixel array.

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